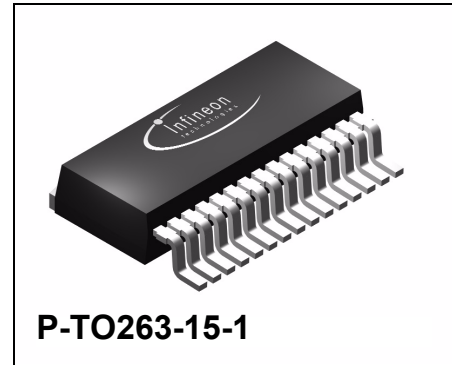


Data Sheet
1 Overview
1.1 Features

- Quad D-MOS switch
- Free configurable as bridge or quad-switch
- Optimized for DC motor management applications
- Low $R_{DS\ ON}$: 26 m Ω high-side switch, 14 m Ω low-side switch (typical values @ 25 °C)
- Maximum peak current: typ. 42 A @ 25 °C
- Very low quiescent current: typ. 4 μ A @ 25 °C
- Small outline, thermal optimized PowerPak
- Load and GND-short-circuit-protection
- Operates up to 40 V
- Status flag for over temperature
- Open load detection in Off-mode
- Overtemperature shut down with hysteresis
- Internal clamp diodes
- PWM capability up to 25kHz
- Cross current free operation up to 13A load current (typ. value @ 12V/150°C)
- Under-voltage detection with hysteresis



Type	Package
BTS 7811K	P-TO263-15-1

1.2 Description

The **BTS 7811K** is part of the **TrilithIC™** family containing three dies in one package: One double high-side switch and two low-side switches. The drains of these three vertical DMOS chips are mounted on separated leadframes. The sources are connected to individual pins, so the **BTS 7811K** can be used in H-bridge- as well as in any other configuration. The double high-side is manufactured in **SMART SIPMOS®** technology which combines low $R_{DS\ ON}$ vertical DMOS power stages with CMOS control circuit. The protected high-side switch contains the control and diagnosis circuit. To achieve low $R_{DS\ ON}$ and fast switching performance, the low-side switches are manufactured in **S-FET 2** logic level technology.

1.3 Pin Configuration
(top view)

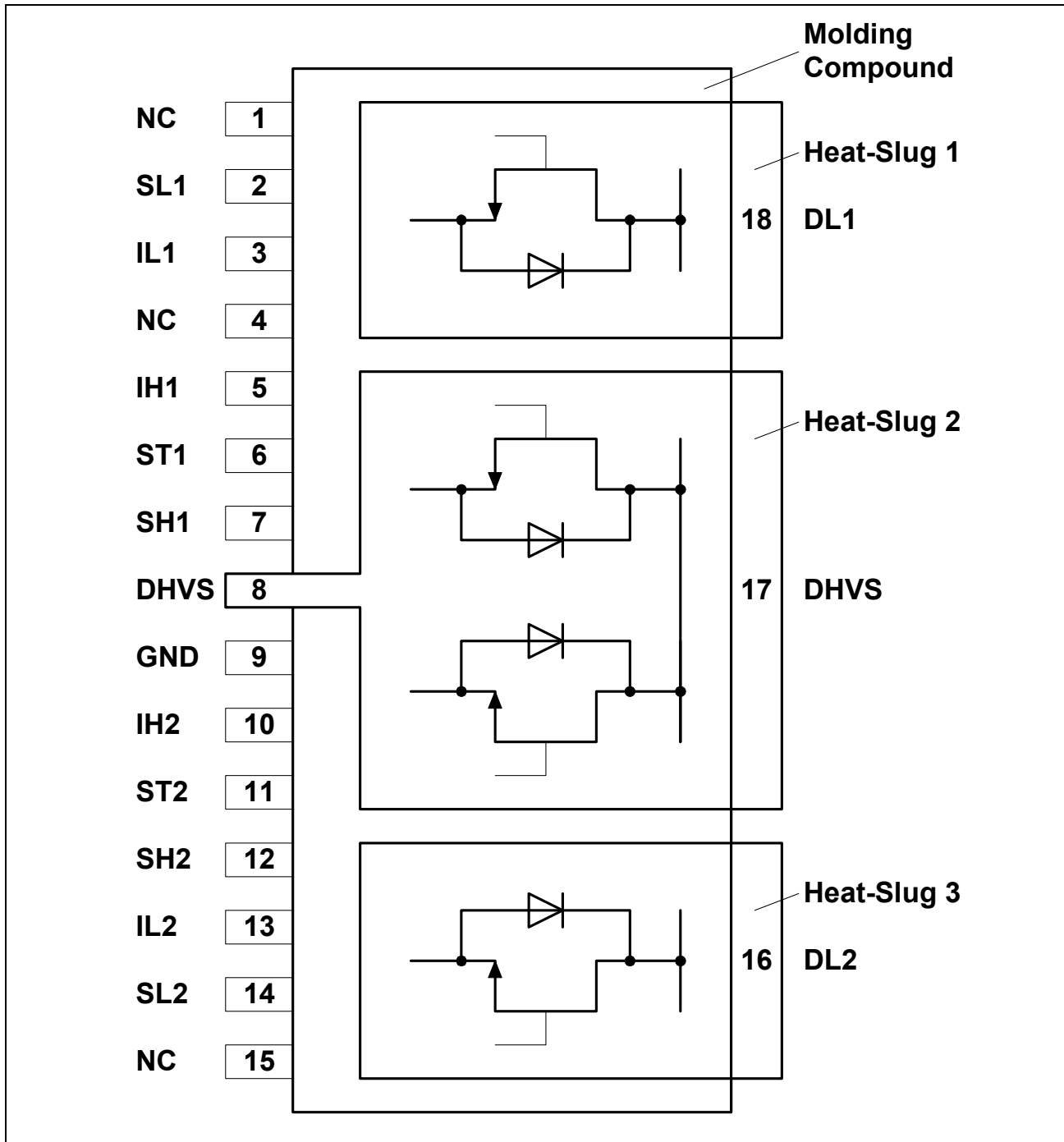


Figure 1: Pin Assignment

1.4 Pin Definitions and Functions

Pin No.	Symbol	Function
1	NC	Not connected
2	SL1	Source of low-side switch 1
3	IL1	Analog input of low-side switch 1
4	NC	Not connected
5	IH1	Digital input of high-side switch 1
6	ST1	Status of high-side switch 1; open Drain output
7	SH1	Source of high-side switch 1
8	DHVS	Drain of high-side switches and power supply voltage
9	GND	Ground of high-side switches
10	IH2	Digital input of high-side switch 2
11	ST2	Status of high-side switch 2; open Drain output
12	SH2	Source of high-side switch 2
13	IL2	Analog input of low-side switch 2
14	SL2	Source of low-side switch 2
15	NC	Not connected
16	DL2	Drain of low-side switch 2 Heat-Slug 3
17	DHVS	Drain of high-side switches and power supply voltage Heat-Slug 2
18	DL1	Drain of low-side switch 1 Heat-Slug 1

Pins written in **bold type** need power wiring.

1.5 Functional Block Diagram

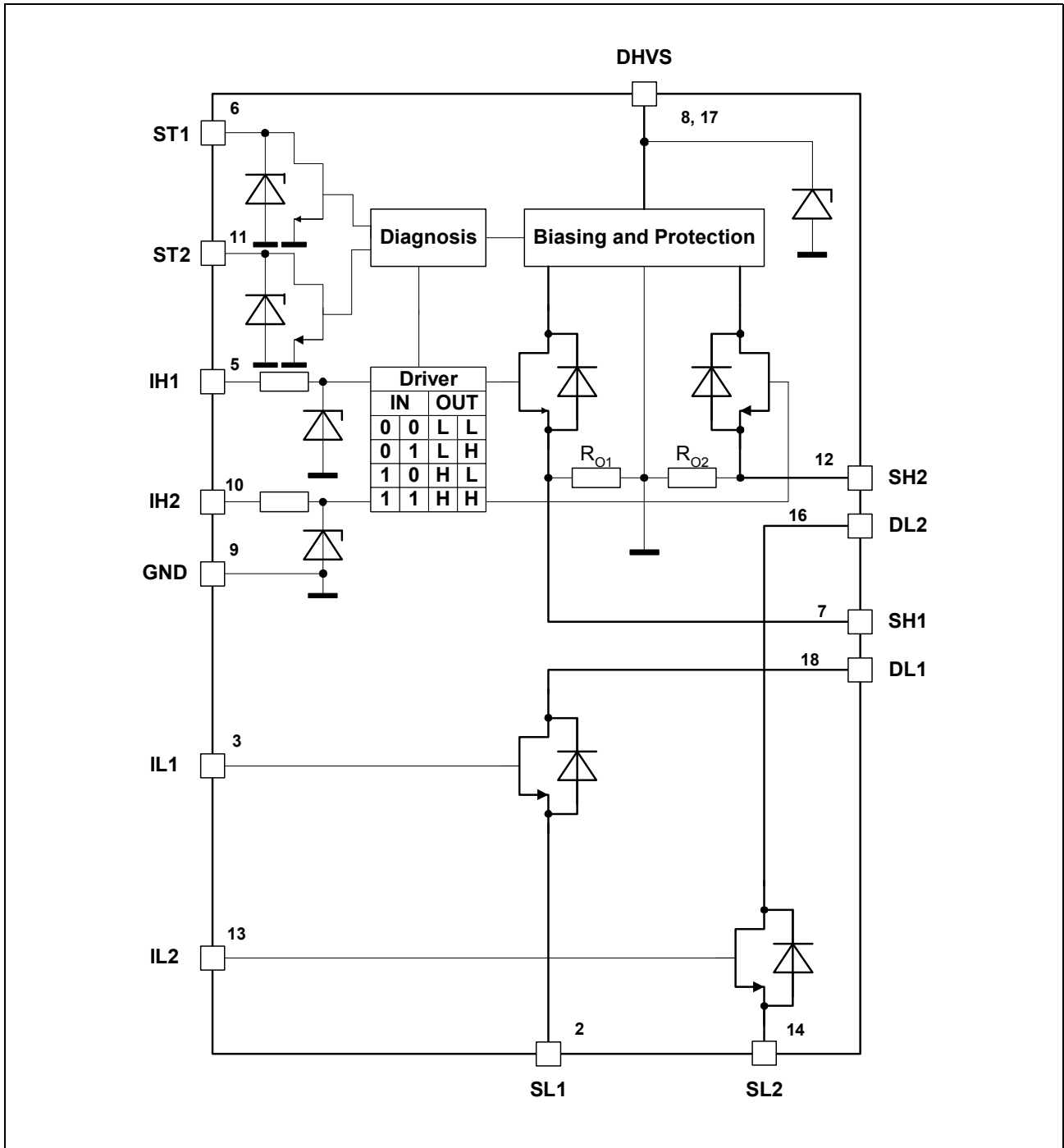


Figure 2: Block Diagram

1.6 Circuit Description

Input Circuit

The control inputs IH1,2 consist of TTL/CMOS compatible Schmitt-Triggers with hysteresis. Buffer amplifiers are driven by these stages and convert the logic signal into the necessary form for driving the power output stages. The inputs are protected by ESD clamp-diodes. The inputs IL1 and IL2 are connected to the gates of the standard N-channel vertical power-MOS-FETs.

Output Stages

The output stages consist of a low $R_{DS\ ON}$ Power-MOS H-bridge. In H-bridge configuration, the D-MOS body diodes can be used for freewheeling when commutating inductive loads. If the high-side switches are used as single switches, positive and negative voltage spikes which occur when driving inductive loads are limited by integrated power clamp diodes.

Short Circuit Protection

The outputs are protected against

- output short circuit to ground
- overload (load short circuit).

An internal OP-amp controls the Drain-Source-voltage by comparing the DS-voltage-drop with an internal reference voltage. Above this trippoint the OP-Amp reduces the output current depending on the junction temperature and the drop voltage.

Overtemperature Protection

The high-side switches incorporate an overtemperature protection circuit with hysteresis which switches off the output transistors and sets the status output to low.

Undervoltage-Lockout (UVLO)

When V_S reaches the switch-on voltage V_{UVON} the IC becomes active with a hysteresis. The high-side output transistors are switched off if the supply voltage V_S drops below the switch off value V_{UVOFF} .

Open Load Detection

The open load detection of the BTS 7811K works in OFF condition and is based on a voltage measurement at the source of the high side switch. In order to use the open load detection a pull up resistor to 5V has to be connected to source of one of the high side switches. Because in ON condition this pull up resistor would connect the bridge output to the μC supply it needs to be disconnected by a transistor when the high side switch is

on. In the data sheet application example (Figure 5) the open load detection would be used the following way:

- Set IH1 = IH2 = LOW (both high side switches off)
- Set IL2 = LOW, IL1 = HIGH (only low side switch 1 is on)
- Connect Rol (open load pull up) to 5V via transistor

If the load is connected properly it will pull down the voltage at SH2 to a value close to 0V. If the load is disconnected the resistor will pull the voltage at SH2 to value close to 5V. If the voltage at SH2 is higher than the open load detection voltage (VOUT(OL)) then ST2 will be pulled down.

Status Flag

The two status flag outputs are an open drain output with Zener-diode which require a pull-up resistor, c.f. the application circuit on page 16. ST1 and ST2 provide separate diagnosis for each high-side switch. Various errors as listed in the table "Diagnosis" are detected by switching the open drain output ST1/2 to low. Forward current in the integrated body diode of the highside switch may cause undefined voltage levels at the corresponding status output. The open load detection can be used to detect a short to Vs as long as both lowside switches are off and R_{OL} is disconnected from 5V by BCR192W.

2 Truthtable and Diagnosis (valid only for the High-Side-Switches)

Flag	IH1	IH2	SH1	SH2	ST1	ST2	Remarks
	Inputs		Outputs				
Normal operation; identical with functional truth table	0	0	L	L	1	1	stand-by mode switch2 active switch1 active both switches active
	0	1	L	H	1	1	
	1	0	H	L	1	1	
	1	1	H	H	1	1	
Open load at high-side switch 1	0	X	Z	X	0	1	detected
	1	X	H	X	1	1	
Open load at high-side switch 2	X	0	X	Z	1	0	detected
	X	1	X	H	1	1	
Overtemperature high-side switch1	0	X	L	X	1	1	detected
	1	X	L	X	0	1	
Overtemperature high-side switch2	X	0	X	L	1	1	detected
	X	1	X	L	1	0	
Overtemperature both high-side switches	0	0	L	L	1	1	detected detected detected
	0	1	L	L	1	0	
	1	0	L	L	0	1	
	1	1	L	L	0	0	
Undervoltage	X	X	L	L	1	1	not detected

*Note: * multiple simultaneous errors are not shown in this table*

Inputs:

0 = Logic LOW

1 = Logic HIGH

X = don't care

Outputs:

Z = Output in tristate condition

L = Output in sink condition

H = Output in source condition

X = Voltage level undefined

Status:

1 = No error

0 = Error

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

$$-40\text{ °C} < T_j < 150\text{ °C}$$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

High-Side-Switches (Pins DHVS, IH1,2 and SH1,2)

Supply voltage	V_S	- 0.3	42	V	-
Supply voltage for full short circuit protection	$V_{S(SCP)}$		28	V	-
HS-drain current	I_S	- 14	*	A	$T_C = 125\text{ °C}$; DC
HS-input current	I_{IH}	- 5	5	mA	Pin IH1 and IH2
HS-input voltage	V_{IH}	- 10	16	V	Pin IH1 and IH2

Note: * internally limited

Status Output ST (Pins ST1 and ST2)

Status pull up voltage	V_{ST}	- 0.3	5.4	V	-
Status Output current	I_{ST}	- 5	5	mA	Pin ST1 or ST2

Low-Side-Switches (Pins DL1,2, IL1,2 and SL1,2)

Drain- source break down voltage	V_{DSL}	55	-	V	$V_{IL} = 0\text{ V}$, $I_D \leq 1\text{ mA}$, $T_j = 25\text{ °C}$
LS-drain current	I_{DL}	-21	26	A	$T_C = 125\text{ °C}$; DC
LS-drain current $T_C = 85\text{ °C}$	I_{DL}	-	42	A	$t_p < 100\text{ ms}$; $v < 0.1$
		-	67	A	$t_p < 1\text{ ms}$; $v < 0.1$
LS-input voltage	V_{IL}	- 20	20	V	Pin IL1 and IL2

Temperatures

Junction temperature	T_j	- 40	150	°C	-
Storage temperature	T_{stg}	- 55	150	°C	-

3.1 Absolute Maximum Ratings (cont'd)

$$-40\text{ °C} < T_j < 150\text{ °C}$$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

Thermal Resistances (one HS-LS-Path active)

LS-junction case	R_{thjCL}	–	1.05	K/W	
HS-junction case	R_{thjCH}	–	1.45	K/W	
Junction ambient $R_{thja} = T_{j(HS)}/(P_{(HS)}+P_{(LS)})$	R_{thja}	–	35	K/W	device soldered to reference PCB with 6 cm ² cooling area

ESD Protection (Human Body Model acc. MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993)

Input LS-Switch	V_{ESD}		0.5	kV	
Input HS-Switch	V_{ESD}		1	kV	
Status HS-Switch	V_{ESD}		2	kV	
Output LS and HS-Switch	V_{ESD}		4	kV	all other pins connected to Ground

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

3.2 Operating Range

$$-40\text{ °C} < T_j < 150\text{ °C}$$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	V_{UVOFF}	42	V	After V_S rising above V_{UVON}
Supply voltage for PWM operation	$V_{S(PWM)}$	8	18	V	–
Input voltages HS	V_{IH}	– 0.3	15	V	–
Input voltages LS	V_{IL}	– 0.3	20	V	–
Status output current	I_{ST}	0	2	mA	–
Junction temperature	T_{jHS}	– 40	150	°C	–

Note: In the operating range the functions given in the circuit description are fulfilled.

3.3 Electrical Characteristics

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$; $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$; $8 \text{ V} < V_S < 18 \text{ V}$
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Current Consumption HS-switch

Quiescent current	I_{SQ}	–	4	9	μA	$I_{H1} = I_{H2} = 0 \text{ V}$ $T_j = 85 \text{ }^\circ\text{C}$
		–	–	20	μA	$I_{H1} = I_{H2} = 0 \text{ V}$
Supply current	I_S	–	4	8	mA	I_{H1} or $I_{H2} = 5 \text{ V}$
		–	8	16	mA	I_{H1} and $I_{H2} = 5 \text{ V}$
Leakage current of highside switch	I_{SHLK}	–	–	7	μA	$V_{IH} = V_{SH} = 0 \text{ V}$ $T_j = 85 \text{ }^\circ\text{C}$, $V_S = 12\text{V}$
Leakage current through logic GND in free wheeling condition	$I_{LKCL} = I_{FH} + I_{SH}$	–	2.2	10	mA	$I_{FH} = 5 \text{ A}$ $V_S = 12\text{V}$

Current Consumption LS-switch

Input current	I_{IL}	–	10	100	nA	$V_{IL} = 20 \text{ V}$ $V_{DSL} = 0 \text{ V}$
Leakage current of lowside switch	I_{DLK}	–	–	12	μA	$V_{IL} = 0 \text{ V}$ $V_{DSL} = 40 \text{ V}$ $T_j = 85 \text{ }^\circ\text{C}$

Under Voltage Lockout (UVLO) HS-switch

Switch-ON voltage	V_{UVON}	–	–	5	V	V_S increasing
Switch-OFF voltage	V_{UVOFF}	1.8	–	4.5	V	V_S decreasing
Switch ON/OFF hysteresis	V_{UVHY}	–	1	–	V	$V_{UVON} - V_{UVOFF}$

3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$; $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$; $8 \text{ V} < V_S < 18 \text{ V}$
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Output Stages

Inverse diode of high-side switch; Forward-voltage	V_{FH}	–	0.8	1.2	V	$I_{FH} = 5 \text{ A}$
Inverse diode of lowside switch; Forward-voltage	V_{FL}	–	0.8	1.2	V	$I_{FL} = 5 \text{ A}$
Static drain-source on-resistance of highside switch	$R_{DS\ ON\ H}$	–	26	35	m Ω	$I_{SH} = 5 \text{ A}$ $T_j = 25 \text{ }^\circ\text{C}$ $V_S = 12\text{V}$
Static drain-source on-resistance of lowside switch	$R_{DS\ ON\ L}$	–	14	17	m Ω	$I_{SL} = 5 \text{ A}$; $V_{IL} = 5 \text{ V}$ $T_j = 25 \text{ }^\circ\text{C}$
Static path on-resistance	$R_{DS\ ON}$	–	–	100	m Ω	$R_{DS\ ON\ H} + R_{DS\ ON\ L}$ $I_{SH} = 5 \text{ A}$; $V_S = 12\text{V}$
Maximum load current for cross current free operation $V_{IL} = 7\text{V}$; $R_{Gate} = 50\Omega$	$I_{L\ max\ ccf}$	5	8	–	A	$V_S > 8\text{V}$, $T_j = 150 \text{ }^\circ\text{C}$
		–	10	–	A	$V_S = 10\text{V}$, $T_j = 150 \text{ }^\circ\text{C}$
		–	13	–	A	$V_S = 12\text{V}$, $T_j = 150 \text{ }^\circ\text{C}$

Note: The device is regarded as cross current free if the reverse flowing charge through the high side switch is less than $1\mu\text{C}$.

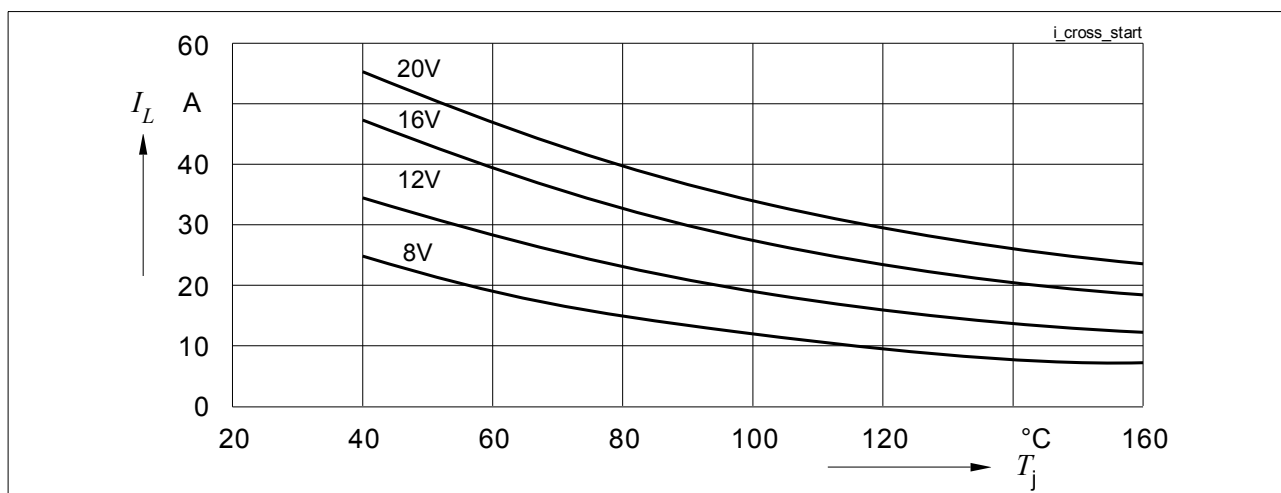


Figure 3: Start of Cross Conduction vs. I_L , V_S and junction Temperature T_j

3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$; $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$; $8 \text{ V} < V_S < 18 \text{ V}$
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Short Circuit of Highside Switch to GND

Initial peak SC current $t_{del} = 150\mu\text{s}$; $V_S = 12 \text{ V}$; $V_{DSH} = 12\text{V}$	I_{SCPH}	35	48	65	A	$T_j = -40 \text{ }^\circ\text{C}$
		–	42	–	A	$T_j = +25 \text{ }^\circ\text{C}$
		25	32	42	A	$T_j = +150 \text{ }^\circ\text{C}$

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions. Protection functions are not designed for continuous or repetitive operation.
 Peak short circuit current is significantly lower at $V_S > 18\text{V}$.

Short Circuit of Highside Switch to V_S

Output pull-down-resistor	R_O	7	14	42	k Ω	$V_{DSL} = 3 \text{ V}$
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Thermal Shutdown

Thermal shutdown junction temperature	T_{jSD}	155	180	190	$^\circ\text{C}$	–
Thermal switch-on junction temperature	T_{jSO}	150	170	180	$^\circ\text{C}$	–
Temperature hysteresis	ΔT	–	10	–	$^\circ\text{C}$	$\Delta T = T_{jSD} - T_{jSO}$

Status Flag Output ST of Highside Switch

Low output voltage	V_{STL}	–	0.2	0.6	V	$I_{ST} = 1.6 \text{ mA}$
Leakage current	I_{STLK}	–	–	5	μA	$V_{ST} = 5 \text{ V}$
Zener-limit-voltage	V_{STZ}	5.4	–	–	V	$I_{ST} = 1.6 \text{ mA}$
Status change after positive input slope with open load ¹⁾	$t_{d(SToffo+)}$	–	–	20	μs	
Status change after negative input slope with open load ¹⁾	$t_{d(SToffo-)}$	–	–	700	μs	

¹⁾Defined by design. Not subject to production test.

3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$; $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$; $8 \text{ V} < V_S < 18 \text{ V}$
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Status change after positive input slope with overtemperature ¹⁾	$t_{d(\text{SToff+})}$	–	1.6	10	μs	$R_{\text{ST}} = 47 \text{ k}\Omega$
Status change after negative input slope with overtemperature ¹⁾	$t_{d(\text{SToff-})}$	–	14	100	μs	$R_{\text{ST}} = 47 \text{ k}\Omega$

Open Load Detection in Off Condition

Open Load Detection Voltage	$V_{\text{OUT(OL)}}$	2	3	4	V	$V_S = 12 \text{ V}$
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Switching Times of High Side Switch

Turn-On-Time to 90% V_{SH}	t_{ON}	–	100	220	μs	$R_{\text{Load}} = 12 \Omega$ $V_S = 12 \text{ V}$
Turn-Off-time to 10% V_{SH}	t_{OFF}	–	120	250	μs	
Slew Rate On 10 to 30% V_{SH}	dV/dt_{ON}	–	0.5	1.1	$\text{V}/\mu\text{s}$	
Slew Rate Off 70 to 40% V_{SH}	$-dV/dt_{\text{OFF}}$	–	0.7	1.3	$\text{V}/\mu\text{s}$	

Switching Times of Low Side Switch

Turn-ON Delay Time ¹⁾	$t_{d(\text{on})}$	–	20	–	ns	resistive load $I_{\text{SL}} = 10 \text{ A}$; $V_{\text{DSL}} = 12 \text{ V}$ $V_{\text{IL}} = 5\text{V}$; $R_{\text{Gate}} = 16\Omega$
Rise Time ¹⁾	t_r	–	85	–	ns	
Switch-Off Delay Time ¹⁾	$t_{d(\text{off})}$	–	60	–	ns	
Fall Time ¹⁾	t_f	–	80	–	ns	

¹⁾Defined by design. Not subject to production test.

3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$; $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$; $8 \text{ V} < V_S < 18 \text{ V}$
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Gate Charge Characteristics

Input to source charge ¹⁾	Q_{IS}	–	4.5	–	nC	$I_{SL} = 10 \text{ A}$; $V_S = 12 \text{ V}$
Input to drain charge ¹⁾	Q_{ID}	–	12	–	nC	$I_{SL} = 10 \text{ A}$; $V_S = 12 \text{ V}$
Input charge total ¹⁾	Q_I	–	30	60	nC	$I_{SL} = 10 \text{ A}$; $V_S = 12 \text{ V}$ $V_{IL} = 0 \text{ to } 5 \text{ V}$
Input plateau voltage ¹⁾	V_{plateau}	–	2.6	–	V	$I_{SL} = 10 \text{ A}$; $V_S = 12 \text{ V}$

Control Inputs of High Side Switches IH1, IH2

H-input voltage	$V_{IH \text{ High}}$	–	–	3.0	V	–
L-input voltage	$V_{IH \text{ Low}}$	1	–	–	V	–
Input voltage hysteresis	$V_{IH \text{ HY}}$	–	0.5	–	V	–
H-input current	$I_{IH \text{ High}}$	5	30	65	μA	$V_{IH} = 5 \text{ V}$
L-input current	$I_{IH \text{ Low}}$	5	14	25	μA	$V_{IH} = 0.4 \text{ V}$
Input series resistance	R_I	2.7	4	6	k Ω	–
Zener limit voltage	$V_{IH \text{ Z}}$	5.4	–	–	V	$I_{IH} = 1.6 \text{ mA}$

Control Inputs IL1, IL2

Gate-threshold-voltage $I_{DL} = 1 \text{ mA}$	$V_{IL \text{ th}}$	–	1.9	3.0	V	$T_j = -40 \text{ }^\circ\text{C}$
		–	1.7	–		$T_j = +25 \text{ }^\circ\text{C}$
		0.8	1.1	–		$T_j = +150 \text{ }^\circ\text{C}$

¹⁾ Defined by design. Not subject to production test.

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25 \text{ }^\circ\text{C}$ and $V_S = 12 \text{ V}$.

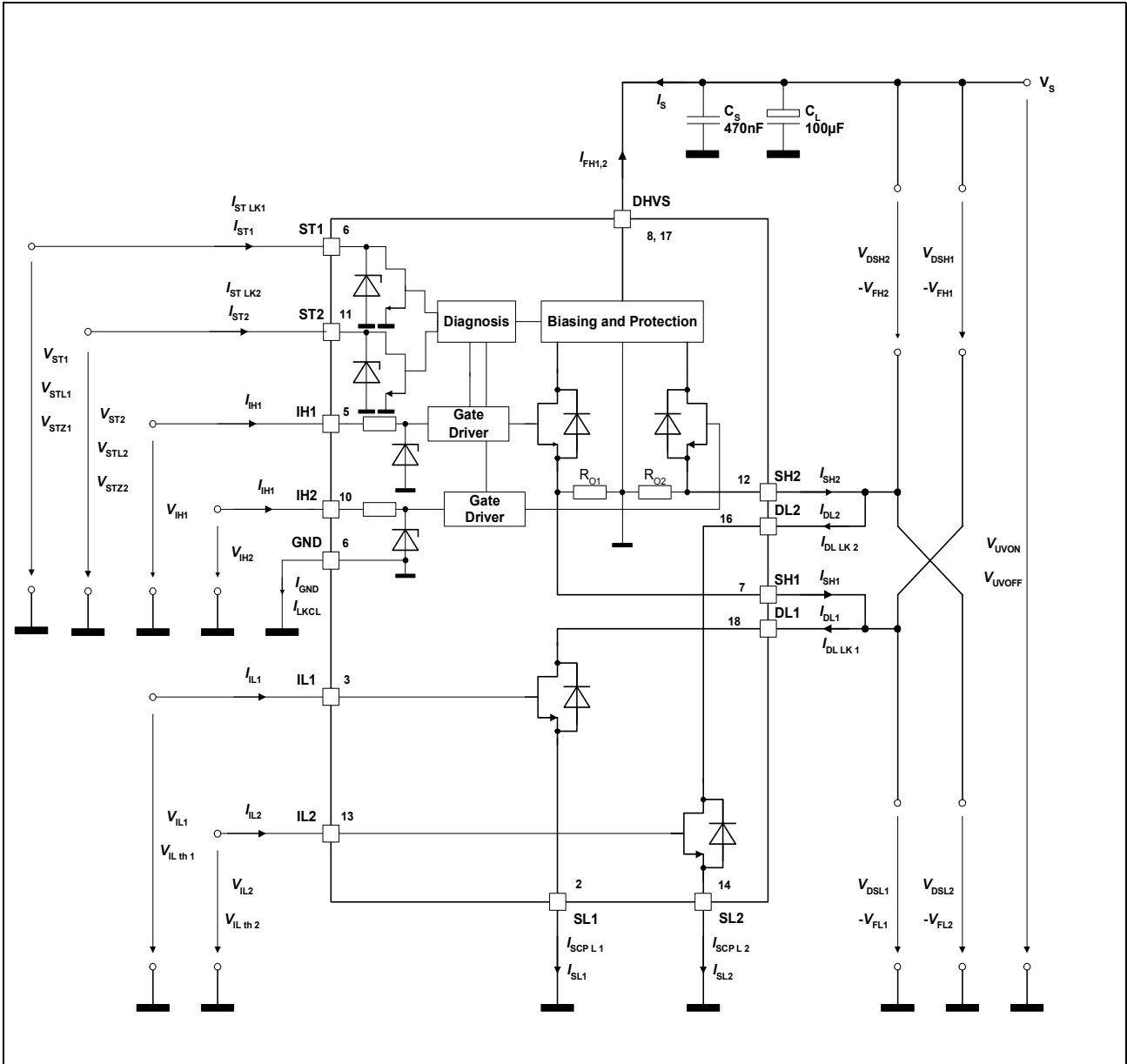


Figure 4: Test Circuit

HS-Source-Current	Named during Short Circuit	Named during Leakage-Cond.
$I_{SH1,2}$	$I_{SCP H}$	$I_{DL LK}$

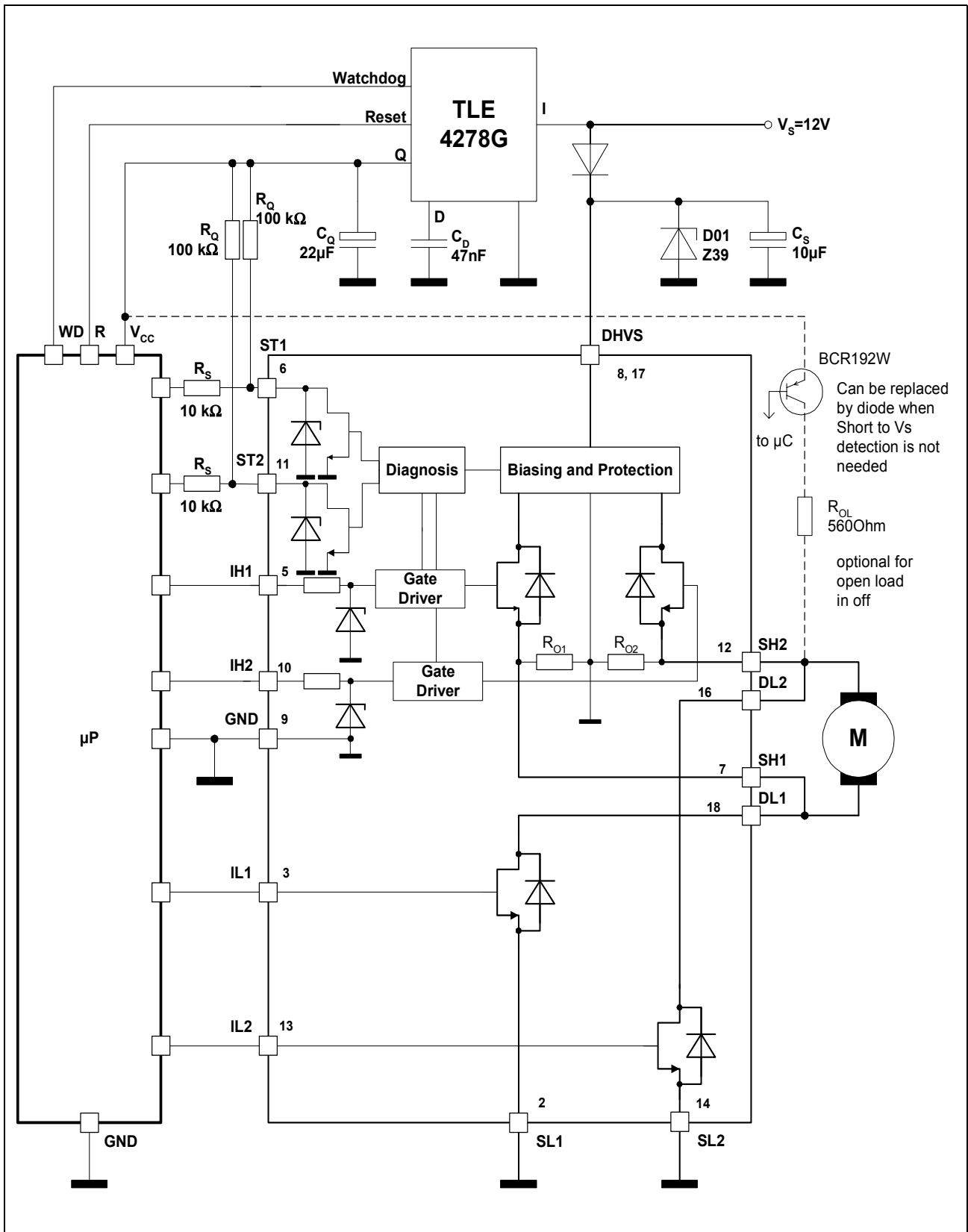
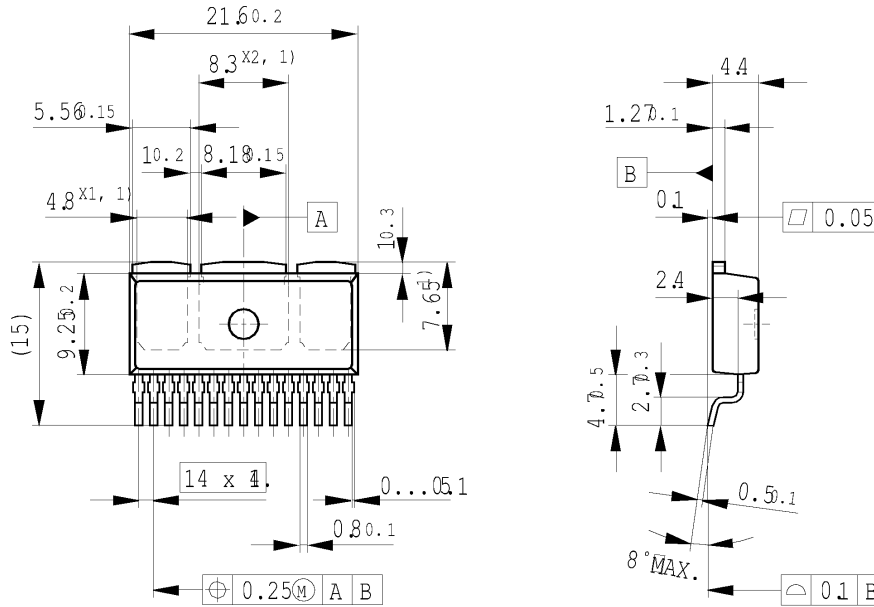


Figure 5: Application Circuit

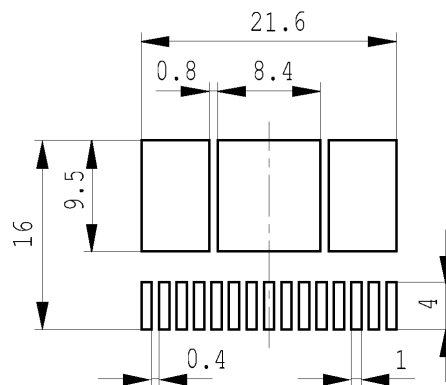
4 Package Outlines

P-TO263-15-1 (Plastic)



- 1) Typical
 Metal surface min. X1 = 3.57, X2 = 9.03, Y = 6.
 All metal surfaces tin plated, except area of cut

Footprint



Sorts of Packing

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/packages..>

SMD = Surface Mounted Device

Dimensions in mm

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